IN THE CLAIMS:

Claims 2, 3, 11 and 12 were previously cancelled. Claims 4, 5, 9, 10, 15, 16 and 21 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Previously presented) A DRAM circuit comprising:

a substrate having an active region thereon and a capacitor structure disposed above the active region, the capacitor structure including a storage node, a dielectric layer overlying the storage node, and a conductive cell plate overlying the dielectric layer, each of the dielectric layer and the conductive cell plate having an end portion proximate a conductive contact, the conductive contact extending downward and adjacently beside the capacitor structure, the end portion of the dielectric layer extending closer to the conductive contact than the end portion of the conductive cell plate;

a first TEOS layer disposed proximate the storage node;

a second TEOS layer disposed over the capacitor structure and encasing the end portions of the dielectric layer and the conductive cell plate, the second TEOS layer disposed between the capacitor structure and the conductive contact; and

a doped BPSG layer disposed over the second TEOS layer, the conductive contact extending through the BPSG layer and the second TEOS layer.

2. (Cancelled)

3. (Cancelled)

4. (Currently amended) The DRAM circuit of claim 1, wherein each of the storage node and the conductive cell plate ~~are~~ is heavily doped with dopants.

5. (Currently amended) The DRAM circuit of claim 1, wherein each of the storage node and the conductive cell plate ~~comprise~~ comprises a phosphorous-doped polysilicon.

6. (Previously presented) The DRAM circuit of claim 1, wherein the dielectric layer comprises a capacitor cell dielectric layer.

7. (Previously presented) The DRAM circuit of claim 1, wherein the dielectric layer comprises a nitride layer.

8. (Previously presented) The DRAM circuit of claim 1, wherein the capacitor structure comprises a container-shaped capacitor.

9. (Currently amended) The DRAM circuit of claim 1, wherein the second TEOS layer is a dopant barrier between the capacitor structure and ~~said~~ the BPSG layer.

10. (Currently amended) A semiconductor memory device comprising:

a semiconductor substrate having an active region thereon and a capacitor structure formed above the active region, the capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, the dielectric layer disposed between the first and second conductive layers, each of the dielectric layer and the first and second conductive layers having an end portion proximate a conductive contact, the conductive contact extending downward and adjacently beside the capacitor structure, the end portion of the dielectric layer extending closer to the conductive contact than the end portion of each of the first conductive layer and the second conductive layer;

a diffusion barrier proximate the first ~~conducting~~ conductive layer and configured to prevent diffusion of contaminants into the active region;

a TEOS layer disposed over the capacitor structure and encasing the end portions of the dielectric layer and each of the first conductive layer and the second conductive layer, the TEOS layer disposed between the capacitor structure and the conductive contact; and

a doped BPSG layer disposed over the TEOS layer, the conductive contact extending through the BPSG layer and the TEOS layer.

11. (Cancelled)

12. (Cancelled)

13. (Previously presented) The device of claim 10, wherein the conductive contact comprises at least one of metal and conductively doped polysilicon.

14. (Previously presented) The device of claim 10, wherein the conductive contact comprises a digit line.

15. (Currently amended) The device of claim 10, wherein each of the first conductive layer and the second conductive layer ~~are~~ is heavily doped with dopants.

16. (Currently amended) The device of claim 10, wherein each of the first conductive layer and the second conductive layer ~~comprise~~ comprises a phosphorous-doped polysilicon.

17. (Previously presented) The device of claim 10, wherein the dielectric layer comprises a capacitor cell dielectric layer.

18. (Previously presented) The device of claim 10, wherein the dielectric layer comprises a nitride layer.

19. (Previously presented) The device of claim 10, wherein the capacitor structure comprises a container-shaped capacitor.

20. (Previously presented) The device of claim 10, wherein the TEOS layer is a dopant barrier between the capacitor structure and the BPSG layer.

21. (Currently amended) The DRAM circuit of claim 1, wherein the first TEOS layer is configured to prevent diffusion of contaminants into the active ~~regions.~~ region.

22. (Previously presented) The DRAM circuit of claim 1, wherein the first TEOS layer comprises a thickness of about 100 Å to about 250 Å.

23. (Previously presented) The semiconductor memory device of claim 10, wherein the diffusion barrier comprises a nitride layer or TEOS layer.

24. (Previously presented) The semiconductor memory device of claim 10, wherein the diffusion barrier comprises a thickness of about 100 Å to about 250 Å.